

REMARKS

Claims 1-6 and 18-22 are currently pending in the application. Claims 13-15 have been canceled, Claims 16 and 17 were previously canceled and Claims 7-12 are currently withdrawn from prosecution. Applicants respectfully request that Claims 7-12 be reinstated, as allowability of Claim 1 indicates the allowability of Claims 7-12 that depend from Claim 1. On the Office Action Summary sheet, Claims 2-6 are not indicated as "objected to", but Applicants presume that they are objected to as indicated in the Office Action and would be allowable if re-written in independent form.

1. Rejection under 35 U.S.C. §102(b)

The Primary Examiner has rejected Claims 1 and 18-22 under 35 U.S.C. §102(b) as being anticipated by Andoh. Applicants respectfully disagree, but have Amended Claims 1 and 18 to more particularly point out features of the present invention. As pointed out in the Remarks submitted in the Amendment filed on June 3, 2004, Andoh does not teach an interface circuit including a receiver for detecting a binary state of a single-ended data signal in conformity with the common-mode voltage of a differential data signal pair, as recited in Claim 1 and the method of operation of which is recited in Claim 18.

The Examiner indicated in the Telephonic Interview

documented above that a rejection under 35 U.S.C. §102 can be issued if a Prior Art structure is deemed "capable of performing the function(s)" recited in the rejected claims (as well as including all recited structural limitations). Applicants respectfully disagree, as support for a teaching or suggestion of functionality recited in the rejected Claims must be evident in the applied references. Otherwise, the analysis of a prior art structure under the above-stated test of whether or not the prior art structure is "capable of performing the functions(s)" amounts to the use of hindsight of the invention to bootstrap an analysis of the prior art. Such an analysis, if used as a standard for rejection, would render unpatentable otherwise novel and patentable uses for existing technology as well as novel applications of existing structures to unforeseen environments.

Further, the Primary Examiner has stated that the rejection under 35 U.S.C. §102(b) is supported by the principle that "all of the recited functional limitations of the claims will be inherent in the operation of Andoh et al's Fig. 1 circuitry *when a data input is applied to the gate terminal of FET11*" (italics added for emphasis). Applicants respectfully disagree. As Andoh does not teach or suggest using the circuit of Figure 1 to receive a single-ended data signal and thereby detect a binary state in conformity with a received differential pair, the Primary Examiner has applied hindsight of the present invention

to Andoh in order to cause the circuit of Andoh to perform the functions recited in Claim 1. Andoh teaches common mode compensated operational amplifiers, not interface circuits using comparators to perform data detection and further does not teach or suggest the use of a unique comparator configuration or circuit to detect the binary state of a single-ended data signal in conformity with the common-mode value of a differential data signal pair. Nor does Andoh suggest such an application of data signals to the inputs of the circuits taught by Andoh. Further, Andoh teaches away from the use of the circuit cited by the Examiner (feedback circuit 13 of Figure 1 of Andoh), as the terminals connected to that circuit are the outputs of the op-amp shown on the left-hand side of the diagram, and not digital signals provided over an interface.

However, applicants have included the differential comparator of Amended Claim 1 in accordance with the Amendment proposed in the Telephonic Interview described above. Previous Claim 2, which was found to be allowable by the Primary Examiner in the previous Office Action if re-written in independent form, included both a differential comparator and a singlential comparator serving as the receiver. In the Telephonic Interview, the Examiner indicated that inclusion of the differential comparator into Claim 1 would distinguish the invention over Andoh. Andoh, even as applied by the Primary Examiner, does not perform the recited functions of detecting the binary states of

both the single-ended signal and the differential data signal pair, and does not structurally include both a circuit for detecting the binary state of the single ended data signal and a differential comparator for detecting the binary state of the differential data signal pair. As the differential data signal pair is read in the rejection by the Primary Examiner onto signals 6 and 7 of Figure 1 of Andoh, there is no differential comparator provided by Andoh for detecting a binary state of signals 6 and 7, which Applicants further point out are not data signals having a binary state at all, but are output signals of an op-amp providing analog voltages to compensation circuit 13.

Similarly, Claim 18 recites "detecting a value of said single-ended data signal in conformity with a common-mode value of said received differential data signal pair, wherein said detected value is representative of a digital binary state of said single-ended data signal." As pointed out above, Andoh does not teach or suggest detection of a data signal binary value at all and therefore does not anticipate the method of Claim 18. However, Applicants have included a further step of detecting the binary state of the differential data signal pair in accordance with the amendment to Claim 1.

Therefore, for all of the reasons stated above, Applicants believe that all of the existing rejections under 35 U.S.C. §102(b) have been overcome.

2. Prospective Rejection under 35 U.S.C. §102(b)

The Primary Examiner has also indicated in the Office Action and in the Telephonic Interview documented above, that Alexander appears to anticipate at least independent Claims 1 and 18. Applicants respectfully disagree. For the same reasons stated above with respect to Andoh, Alexander does not teach a detector as recited in Claim 1 or the detecting step recited in Claim 18, as the circuits disclosed in Andoh are likewise op-amps having a common mode compensation input and not detectors for detecting the binary state of a single-ended signal in conformity with a common-mode value of a differential signal pair. Similarly, an analysis of Alexander that applied such data signals would require the same hindsight as mentioned above with respect to Andoh.

However, even as prospectively applied by the Primary Examiner, the circuit of Figure 4 of Alexander does not perform the functions recited in independent Claims 1 and 18.

Applicants point out that if the circuit of Figure 4 of Alexander were to receive a single-ended data signal at terminal V_{cm} and a differential data signal pair across terminals 37 and 38, that output signals provided at the junction of the drains of transistor pairs 54, 80 and 56, 82 (or at the outputs of the op-amp) would not be representative of binary states of either the single-ended data signal or the differential data signal pair.

First, the single-ended signal would affect both outputs of

the op-amp, and thus the sub-circuits on neither side of the Figure would detect the binary state of the differential pair, as the single-ended signal would change both outputs in accordance with its binary state.

Next, as transistors 52 and 80 (and similarly transistors 58 and 82) are not commonly connected at their drains, the function of the circuit of Figure 4 of Alexander is to amplify the *differential* voltage of the differential pair at the outputs, not to detect a single-ended input in conformity with the *common-mode* voltage of the differential data signal pair. So, referring to Figure 4 of Alexander, if V_{38} is decreased, V_{o-} increases, but if V_{37} is decreased, V_{o-} also decreases, resulting a in dependence on the difference between the differential inputs, as expected for a differential operational amplifier. In order for the circuit to provide detection of the single-ended input in conformity with a common-mode value of the differential inputs, the detection circuit would need to be symmetrical with respect to the differential inputs, as the common mode voltage of the differential pair is the average voltage, which is symmetrical with respect to each signal. Each side of the circuit in Figure 4 of Alexander is asymmetrical with respect to the differential input pair and so, for example if V_{37} is set to 1 Volt and V_{38} is set to 3V, the resulting output of either side is not the same for a given V_{cm} as if V_{37} is set to 3 Volt and V_{38} is set to 1V - a

requirement if the circuit is to act in conformity with the common mode voltage of the differential signal pair, which in both cases is 2V.

Terminal V_{cm} is described throughout the specification of Alexander as a terminal for setting the *output* common-mode voltage of the op-amp. (See e.g. Alexander col. 3 lines 38-40.) As such, it is also apparent from the description of Alexander that a signal injected into terminal V_{cm} will not be detected in conformity with the differential pair common-mode voltage, but rather will set the common mode output voltage of a signal representing the difference between the differential inputs. (See Alexander col. 6, lines 14-20 and lines 36-42). Therefore, the circuit of Figure 4 of Alexander does not perform the functions recited in independent Claims 1 and 18.

Therefore, for all of the reasons stated above, applicants believe that Alexander does not anticipate or suggest the present invention as claimed.

3. Provisional double-patenting rejection

The Examiner has issued a provisional double-patenting rejection of Claims 1 and 18-22 under the claims of co-pending application 10/616,012. Applicants respectfully point out that Claims 1 and 18 are claims to an interface rather than a comparison circuit and that the comparison circuit included in the interface of the above-referenced Claims is generic over the claimed embodiment of the above-cited application, due to a Restriction requirement issued in the instant application. Therefore, applicants believe that the provisional double-patenting rejection should be withdrawn.

Therefore, for all of the reasons stated above, applicants believe that all of the rejections and objections have been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Amendment, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1-18 are in condition for allowance. Such action is earnestly solicited.

No fees should be incurred by this Amendment, but if there are any fees incurred by this Amendment Letter, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,



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